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Process-induced strain in silicon-on-insulator materials

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Abstract
We present a detailed investigation of the influence of oxidation and thinning processes on the in-plane stress in silicon-on-insulator materials. Combining double x-ray diffraction, Fourier transformed infrared and micro-Raman spectroscopy, we show that one can separately evaluate the stress present in the silicon over layer, the buried oxide and the underlying (handle) silicon wafer at any time of a device-forming process.

1. Introduction

Applications of silicon-on-insulator (SOI) technology have long been limited to space and military programmes in which radiation hardness is more important than performance and cost. The benefits of SOI as a substrate material for applications such as high-end logic, microprocessors and low-power devices for portable applications became apparent only at the 0.18 μm technology node. As a consequence, during the past two years an increasing number of IC manufacturers have moved into production of partially depleted (PD) MOS devices on SOI. As the IC feature size continues to shrink down to 0.10 μm, device technology is moving further from PD to fully depleted (FD) silicon layers. Translated into SOI wafer requirements, this means having a decreased silicon overlayer (SOL) thickness. In this case, the evaluation (and control) of stress and strain in the thin silicon film becomes a central problem.

In bulk silicon and SOI, the strain originates mainly from the difference in specific volume between Si and SiO_2 [1] and acts contractively on the active part of the device located between two local or field oxides (the so-called LOCOS or FOX in Si technology). For SOI wafers, Kimura and Ogura [2] showed that the LOCOS process may introduce very large source of stress (as large as 500 MPa). In this case, the mechanical properties of the surrounding oxide influence not only the transport properties of the electrons in the conduction channel of the

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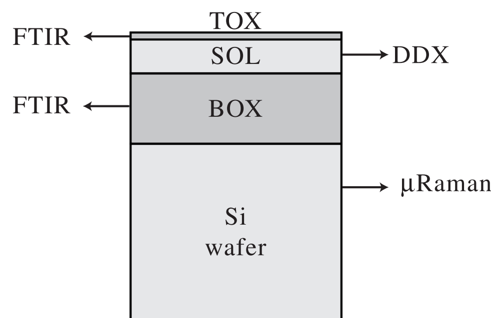

Figure 1. A schematic drawing of an oxidized SOI wafer. The top oxide layer is labelled as TOX, the silicon over layer as SOL and the buried oxide as BOX. The bottom layer is the handle silicon wafer. We used micro-Raman spectroscopy to determine the strain present in the handle wafer; FTIR spectroscopy to estimate roughly the strain in the oxide films and to control the thicknesses of the different layers; and x-ray diffraction to determine the strain in the thin, active SOL.

transistors but also the gate oxide properties. In 1990, Bjorkman *et al* [3] evidenced a linear relationship between the mid-gap interface state density and the thickness-averaged stress and strain in thermally grown oxides. The stress present in the gate oxide also affects the leakage current, which increases as the oxide thickness decreases [4–6]. Negative reports have also been given concerning the reduced device mobility and increased defectiveness.

In a recent paper [7] Camassel *et al* investigated the residual strain (and residual strain relaxation) in SOI wafers subjected to different thinning processes. From detailed micro-Raman experiments, they showed that

(i) the strain depends on every step of the technology and
(ii) relaxes uniformly in the underlying (handle) silicon wafer on a scale of several microns (2–3 μm).

Because of the finite size of the micro-Raman probe, much less was found out about the strain present in the SOL and oxide. In this work, we report a combined and detailed study on the influence of oxidation and thinning on the residual stress in SOI wafers.

2. Experimental techniques

Standard SOI is made of a thin (200 nm) SOL on top of a buried oxide (BOX) film. The typical BOX is 400 nm thick and, below this topmost sandwich, there is a thick handle silicon wafer (figure 1). The SOI-forming process requires a high-temperature annealing step which usually induces some residual (thermal) biaxial strain in the SOL, BOX and handle wafer [7, 8]. The strain is tensile in the SOL and handle wafer; it is compressive in the BOX. In this work we used as starting materials two standard bonded SOI wafers [9]. The first (a) was used to study the influence of oxidation. The second (b) was progressively thinned by wet sacrificial oxidation down to 10 nm.

We used double x-ray diffraction to measure the stress present in the SOL [2]. We used Fourier transformed infrared (FTIR) spectroscopy to probe the thickness and refractive index of every participating layer and to estimate the average stress in the oxide films [3, 10]. We used micro-Raman spectroscopy to determine the strain, and strain relaxation, in the handle wafer [7]. For an exhaustive review of the use of micro-Raman spectroscopy to investigate local mechanical stress in silicon integrated circuits, we refer to the reader the work of Ingrid De Wolf [11].

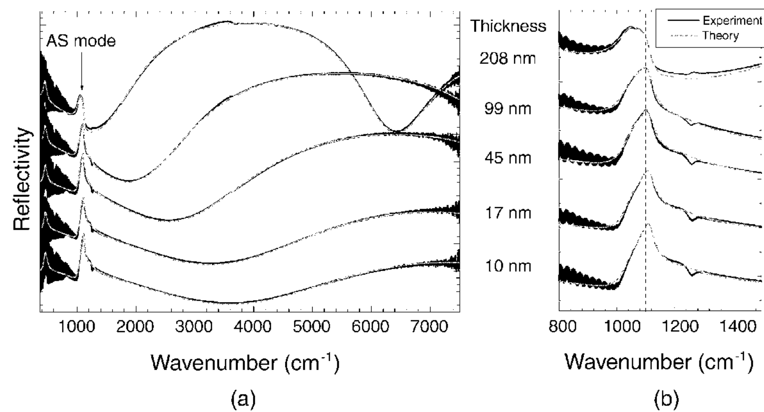

Figure 2. (a) FTIR spectra of a SOI wafer progressively thinned by wet sacrificial oxidation. The experimental (simulated) spectra are plotted as a full black (grey) line. From the interference pattern at high frequency (2000–7500 cm^{-1}), we deduce the refractive index and thickness of each layer. (b) From the frequency shift of the AS infrared mode of SiO_2 we estimate the average stress in the oxide.

3. Oxidation

We first applied our threefold investigation scheme (using FTIR, DDX and micro-Raman spectroscopy) to the nominal SOI material. To extract precisely the thicknesses of the different layers and the exact SiO_2 mode frequencies, we simulated the infrared spectra with a model based on optical transfer matrix technique [12–14]. We calculated the dielectric constant of the oxide with the factorized form of the Lorentz model with three oscillators [15, 16] and got the results shown in figure 2. Notice the excellent agreement between the simulated and experimental reflectivity spectra.

From the high-frequency interference pattern, we deduced the refractive index and thickness of every layer. From the strong absorption line near 1075 cm^{-1} (figure 2(b)) we deduced the average stress in the oxide. This is an asymmetrical stretching (AS) vibration in which the oxygen atom moves back and forth along a line parallel to the axis joining the two silicon atoms. Its frequency is very sensitive to the variation of the Si–O–Si bond angle θ [10, 17–19], and, as the compression expresses itself in the oxide as a decrease of θ [20, 21], a careful study of the As infrared mode gives a direct image of the stress and stress gradient present in the oxide [3, 10]. Stress values obtained for the BOX are gathered in table 1.

We find that the nominal BOX compression can reach −290 MPa. At the same time, micro-Raman spectroscopy shows that the stress present in the handle wafer is tensile and maximum at the Si/SiO_2 interface (175 MPa) but relaxes on a scale of 2 μm [7]. The SOL is also in tensile stress but the DDX rocking curve shows that the magnitude is smaller (about 2.3 MPa).

After oxidation, the top oxide (TOX) is 57 nm thick, the SOL thickness reduces to 178 nm and the BOX remains constant. The important point is that, despite a very small thickness difference, the addition of this second source of strain changes the mechanical state of the whole structure drastically. The stress in the SOL (35 MPa) is 15 times higher; the stress in the wafer becomes 450 MPa. The stress present in the oxides stays approximately constant (−300 MPa). We could not discriminate between the stress level in the BOX and TOX and assumed identical values in the two cases. This approximation is not satisfactory, but etching

Table 1. Effects of the SOL thinning on the biaxial stress (MPa) in the SOL and BOX. The stress is tensile in the SOL and compressive in the BOX. When the SOL is thinned, the BOX relaxes its compressive stress state. Therefore the stress increases in the SOL. The values of SOL stress, when the SOL is thinner than 30 nm, were extrapolated from measured ones using σ (MPa) $= 654\,e^{-1}$, e being the SOL thickness expressed in nm.

	TOX thickness (nm)	SOL thickness (nm)	SOL stress (MPa)	BOX stress (MPa)
Nominal	—	205	2.3	−290
Oxidized	57	178	35	−300
Thinned	—	99	5.4	−170
	—	45	18.7	−140
	—	17	38.5	−100
	—	10	65.4	∼0

the TOX would affect the stress present in the remaining layers, and therefore cannot be used to get additional data about the strain difference.

4. Thinning a SOI wafer

After thinning the nominal SOI wafer (b) by sacrificial oxidation, FTIR, DDX and micro-Raman spectra were again collected. A comparison of FTIR and simulated spectra for the full series of samples is shown in figure 2. In figure 2(b), we focus on the shift of the AS mode to high frequency. It shows the progressive relaxation of the BOX compressive stress. Stress values are gathered in table 1. This relaxation also induces an increase of the in-plane stress in the silicon layers. In the handle wafer, this stress variation cannot be quantitatively estimated, because it is manifested by a broadening of the Si Raman mode and not a homogeneous shift. It traduces an increase of the stress gradients and of the strain fluctuations near the Si/SiO_2 interface [7].

From the DDX rocking curves, we could measure the tensile stress present in SOL with thickness larger than 30 nm. When the SOL is too thin, the SOL rocking curve is weak and hidden by the noise. In order to estimate the stress in the very thin SOI wafers, we extrapolated the measured values using

$$\sigma\ (\text{MPa}) = \frac{654}{e} \quad (1)$$

where σ is the SOL biaxial stress and e the SOL thickness expressed in nanometres. Measured and extrapolated values of the biaxial stress as a function of SOL thickness are shown in figure 3. Notice that the extrapolated stress (131 MPa) for a 5 nm thick active layer is one order of magnitude smaller than the tension involved in silicon deposited on $Si_{0.8}Ge_{0.2}$ (1.3 GPa).

Finally, AFM measurements evidence the existence of a critical thickness near 40 nm. The SOL surface roughness (which is related to strain fluctuations near the silicon oxide interfaces) indeed increases drastically when the SOL becomes thinner than 40 nm. It starts from 1.5 Å RMS and reaches 4 Å for the thinner sample [22].

5. Conclusions

To summarize, we have confirmed that SOI is not at all a perfectly strain-relaxed system but behaves like a balanced-strain structure. When the SOL is progressively thinned by sacrificial

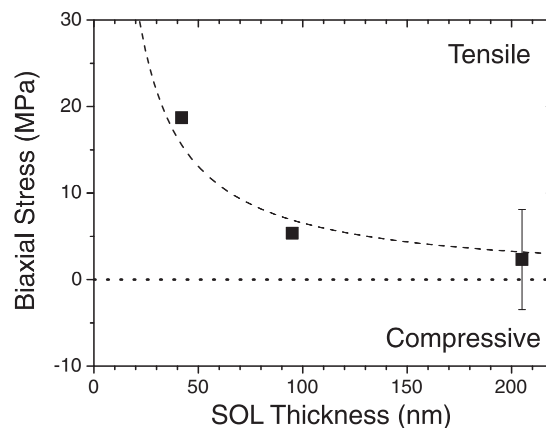

Figure 3. In-plane stress in the thin active film of SOI wafers as a function of SOL thickness. The black squares represent the measured values, the dashed line their extrapolation.

oxidation, the BOX relaxes and the tensile stress increases in the SOL and the handle wafer. Moreover, the SOL surface roughness increases. As a consequence, thinning a nominal SOI wafer is not an easy way to produce a thin SOI wafer for FD MOS technology. The SOI wafer must instead be produced directly with a thin silicon overlayer either with wafer bonding techniques or with a low-dose/low-energy oxygen implantation.

The SOL oxidation induces strong stress variation in the SOI wafer. After growing a thin (57 nm) oxide layer on a nominal SOI wafer, we find that the average in-plane stress in the active layer is 15 times higher. This is still far from the values of the order of a GPa involved in some cases for defective devices [5, 6], but shows that such catastrophic values can be easily achieved due to inappropriate device processing or design. In a recent work [23], we estimated the effect of As implantation on the stress in SOI wafers. We found that the introduction of interstitial As atoms in the silicon crystal induces a strong compressive stress in the SOL (−193 MPa for the highest dose) which also compresses the BOX (−920 MPa). Fortunately, after appropriate annealing, we found that many effects of the process relax.

Acknowledgments

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